In the Claims:

1. (Currently Amended) A data processing system having:

at least one processor chip including a processor unit and an internal data cache, and

an interface external to the internal data cache and external to the processor chip, and configured to receive cache mirror data from the processor chip, wherein

the cache mirror data comprises all data written to the internal data cache, and

the interface is further configured to discard all the cache mirror data designated to be written to an external memory received from the processor chip so that the cache mirror data ~~any of the data written to the internal data cache~~ is never written to any external memory during operation of the processor chip.

2. (Previously Presented) A data processing system according to claim 1 in which the interface is coupled to a memory, the interface passing data to the processor chip during initialization.

3. (Original) A data processing system according to claim 1 further including one or more further processing chips which have read/write access to external memory.

4. (Currently Amended) A method of operating a processing chip having a processor, an internal data cache and a cache controller for transmitting cache mirror data write instructions out of the processing chip, the method including discarding the write instructions designated for an external memory at an interface external to the processing chip so that [[any]] cache mirror data comprising all data written to the internal data cache is never written to any external memory during operation of the processing chip, the external interface providing a connection between

the processing chip and an address controller; and arranging for the program code operated by the processor to require only the data cache as memory.

5. (Previously Presented) A data processing system according to claim 1 wherein the at least one processor chip comprises exactly one processor chip.

6. (Previously Presented) A data processing system according to claim 1 wherein the at least one processor chip comprises two processor chips.

7. (Previously Presented) A data processing system according to claim 1 wherein the processor chip further includes an internal cache controller coupled between the internal data cache and the processor unit.

8. (Currently Amended) A data processing system comprising:

a processor chip including an internal processor coupled to an internal data cache;

an external memory;

an address decoder; and

an interface external to the internal data cache and external to the processor chip, the interface coupled between the processor chip and the external memory and providing the only connection between the processor chip and the address decoder, wherein

the interface is configured to receive memory data from the external memory and transfer the memory data to the processor chip, and

the interface is further configured to

receive internal data cache mirror data from the processor chip, internal cache mirror data comprising all data written to the internal data cache, and

discard all the internal data cache mirror data designated to be written to the external memory so that ~~any of the data written to the internal data cache~~ the internal cache mirror data is never written to any external memory.

9. (Previously Presented) The system of claim 8 and further comprising a control circuit coupled to the interface circuit, the control circuit providing a control signal to indicate whether data received by the interface should be discarded.

10. (Previously Presented) The system of claim 9 wherein the control circuit comprises a decoder.

11. (Previously Presented) The system of claim 8 and further comprising:
a second processor chip that includes an internal processor coupled to an internal cache; and
a second interface, wherein the second processor chip is coupled to the external memory through the second interface.

12. (Previously Presented) The system of claim 11 and further comprising a system bus coupled to the processor chip, the second processor chip, the interface, and the second interface.

13. (Previously Presented) The system of claim 12 and further comprising a third processor chip coupled to the system bus.

14. (Previously Presented) The system of claim 13 wherein the third processor chip comprises a master processing unit and wherein the processor chip and the second processor chip comprise slave processing units.

15. (Previously Presented) The system of claim 14 and further comprising a second external memory directly coupled to the system bus.

16. (Currently Amended) A method of operating a data processing system having a plurality of integrated circuits, each integrated circuit having a processor, an internal data cache, and a cache controller, the method comprising:

transmitting first cache mirror data write instructions designated to an external memory interface from a first cache controller of a first integrated circuit, wherein the external memory interface is located outside the first integrated circuit, wherein first cache mirror data write instructions comprise instructions to write first cache mirror data, the first cache mirror data comprising all data written to an internal data cache of the first integrated circuit; and

discarding the first cache mirror data write instructions from the first cache controller of the first integrated circuit at the external memory interface so that the first cache mirror data ~~any of the data written to the internal data cache of the first integrated circuit~~ is never written to any external memory during operation of a first processor on the first integrated circuit.

17. (Previously Presented) The method of claim 16, further comprising:

transmitting second cache mirror data write instructions from a second cache controller in a second integrated circuit to the external memory interface; and

writing the second cache mirror data write instructions from the external memory interface to external memory.

18. (Previously Presented) The method of claim 17, further comprising:

determining if a task requires a read/write memory that is larger than an internal data

cache size; and

allocating the task to the first integrated circuit or to the second integrated circuit based upon the determining step.

19. (Previously Presented) The data processing system of claim 1, wherein the cache mirror data is designated to be written to an external memory by a write command from the at least one processor chip to the external memory.

20. (Currently Amended) The data processing system of claim 1, wherein the ~~first~~ cache mirror data is designated to be written to an external memory by transmitting the ~~first~~ cache mirror data on an external interface bus coupled to the at least one processor chip and the interface.

21. (Previously Presented) The method of claim 4, wherein transmitting cache mirror data further comprises transmitting a write command from the processing chip to the external interface to designate the cache mirror data for the external memory.

22. (Previously Presented) The method of claim 4, wherein transmitting the cache mirror data out of the processing chip comprises transmitting the cache mirror data on an external interface bus coupled between the external interface and the processing chip.

23. (Previously Presented) The system of claim 8, wherein the internal data cache mirror data is designated to be written to an external memory by a write command from the processor chip to the external memory.

24. (Previously Presented) The data processing system of claim 8, wherein the internal data cache mirror data is designated to be written to an external memory by transmitting the internal data cache mirror data on a system bus coupled to the processor chip and the interface.

25. (Previously Presented) The method of claim 16, wherein transmitting the first cache mirror data further comprises transmitting a write command from the first processor on the first integrated circuit to the external interface to designate the first cache mirror data for the external memory.

26. (Previously Presented) The method of claim 16, wherein transmitting the first cache mirror data out of the first integrated circuit comprises transmitting the cache mirror data on an external interface bus coupled between the external interface and the first integrated circuit.